

# FILM FORMING METHOD IN WHICH FLOW RATE IS SWITCHED

## Background of the Invention

### 1. Field of the Invention

5           The present invention relates to a film forming method using a plasma CVD apparatus for a semiconductor device.

### 2. Description of the Related Art

          There has been arisen a problem of  
10   destruction of a gate oxide film formed by a plasma CVD apparatus with thinning of a pattern in an LSI. Particularly, when a high density plasma (HDP) is used for a filling process of an interline space with a high aspect ratio in a plasma CVD process, a gate  
15   oxide film is often destroyed by electrons or ions in the plasma.

          When an oxide film is formed by use of a conventional plasma CVD apparatus, high frequency power is applied after gases such as  $O_2$ , Ar and  $N_2$  are  
20   introduced into a reaction chamber. Then, when the plasma is stabilized, gases such as  $SiH_4$ ,  $SiF_4$  and TEOS are introduced into the chamber. Alternatively, gases such as  $SiH_4$ ,  $SiF_4$  and TEOS are introduced into the chamber at the same time as the application of the  
25   high frequency power.

          Figs. 2A to 2E are conventional timing charts when gases are introduced into a reaction chamber,

when an oxide film is formed in the following procedure. A wafer is introduced into the chamber and is placed on a stage.  $O_2$  gas is introduced into the chamber, and at the same time Ar gas is introduced into the chamber. After the gas flow rates of the respective introduced gases are stabilized, high frequency power is applied from a high frequency power source to generate a plasma. The generated plasma increases the temperature of the wafer to a temperature in a range of 200 to 400  $^{\circ}C$ . Then,  $SiH_4$  gas is introduced into the chamber. Then, a bias power is applied to the wafer by a high frequency source connected to the stage. The application of the bias power is carried out at the same time as the introduction of the  $SiH_4$  gas into the chamber or after several seconds. The  $SiH_4$  gas is supplied through two pipes and the gas flow rates for the respective pipes are set to different values by mass flow controllers. In particular, the gas flow rate supplied through one pipe is set to a level appropriately between one fifth and one tenth of the gas flow rate supplied through the other pipe.

In this case, the film is initially formed from a region of the wafer where a nozzle of the other pipe is provided, i.e., from a peripheral region of the wafer. Therefore, the film cannot be uniformly formed over the whole wafer surface at the initial

step, and the center region of the wafer has a thinner thickness. In such a situation, when a large amount of electrons and ions are injected on the whole wafer surface, insulating breakdown of a gate oxide film  
5 formed in the center region is deteriorated.

Fig. 5 shows gate breakdown voltages in gate oxide films of transistors prepared by such a film forming technique, when wiring lengths are 320  $\mu\text{m}$ , 20320  $\mu\text{m}$ , 80320  $\mu\text{m}$  and 320320  $\mu\text{m}$ , respectively. In  
10 general, a gate leak current is  $10^{-12}$  A or less in case of the gate voltage of 2.5 V. In the gate oxide film formed by the conventional method, the breakdown voltage is deteriorated and a current larger than  $10^{-12}$  A flows. It would be understood that the  
15 deterioration becomes more serious as the wiring length becomes longer.

In case that an oxide film is formed by the conventional plasma CVD apparatus as mentioned above, the gate oxide film is deteriorated at an initial  
20 stage of the film forming process.

In conjunction with the above description, a CVD method of compound semiconductor is disclosed in Japanese Laid Open Patent Application (JP-A-Heisei 3-150294). In this reference, an epitaxial growth gas  
25 and a doping gas are supplied into a reaction chamber in which a semiconductor substrate is located. In this case, the introduction start timing of the doping

gas is made later than that of the epitaxial growth gas. For example, the doping gas starts to be supplied after at least one molecule layer of a compound semiconductor layer which does not contain  
5 impurity is formed. Thus, the impurity-doped compound semiconductor layer is formed on the semiconductor substrate.

Also, an insulating film used for a semiconductor device is disclosed in Japanese Laid  
10 Open Patent Application (JP-A-Heisei 9-289209). In this reference, a CVD film is formed from material gas containing a gas which has a Si-H coupling as an interlayer insulating film or a passivation film. In this case, a quantity of Si-H couplings in the CVD  
15 film is adjusted to be equal to or less than  $0.6 \times 10^{21}$   $\text{cm}^{-3}$  to restrain the generation of electron traps in a gate oxide film or a tunnel oxide film and to prevent the change of a threshold value of a transistor. Also, a refractive index of the CVD film is adjusted to be  
20 equal to or more than 1.65 or nitrogen concentration in the CVD film is adjusted to be equal to or more than  $3 \times 10^{21}$   $\text{cm}^{-3}$ , for improvement of moisture resistance.

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#### Summary of the Invention

Therefore, an object of the present invention is to provide a film forming method of forming a

plasma oxide film whose breakdown voltage is not deteriorated.

In an aspect of the present invention, a method of forming a film, is attained by (a) starting  
5 supply of a reaction gas at a first flow rate into a chamber in which a plasma is formed, such that an initial film is formed on a wafer; and by (b) starting supply of the reaction gas at a second flow rate into the chamber in which the plasma is formed, after the  
10 step (a), such that the film is formed on the initial film, the first flow rate being smaller than the second flow rate.

Here, the reaction gas may be a compound gas containing Si. In this case, it is desirable that the  
15 reaction gas is one of  $\text{SiH}_4$ ,  $\text{SiF}_4$  and TEOS.

Also, it is desirable that the step (b) is carried out 1 to 10 seconds after the step (a) is carried out.

Also, the first flow rate may be in a range  
20 of one fifth to one tenth of the second flow rate.

Also, in the (a) starting step, the supply of the reaction gas at the first flow rate into the chamber is started via a first nozzle, and the first nozzle may be provided on the chamber above a center  
25 region of the wafer.

Also, in the (b) starting step (b), the supply of the reaction gas at the second flow rate

into the chamber is started via second nozzles, and the second nozzles may be provided on side walls of the chamber above the wafer.

In another aspect of the present invention, a method of forming a film, is attained by (a) forming a film from a center region of a wafer by supplying a reaction gas, while a thickness of the film is equal to or thinner than 10 nm; and by (b) forming the film on whole of the wafer, by supplying the reaction gas, after the step (a).

The (a) forming step may be attained by supplying the reaction gas at a first flow rate, the (b) forming step may be attained by supplying the reaction gas at a second flow rate, and the first flow rate may be in a range of one fifth to one tenth of the second flow rate.

Also, the reaction gas may be a compound gas containing Si, and the reaction gas desirably is one of  $\text{SiH}_4$ ,  $\text{SiF}_4$  and TEOS.

Also, it is desirable that the (b) forming step is carried out 1 to 10 seconds after the step (a) is carried out.

Also, when the (a) forming step is attained by starting supply of the reaction gas at the first flow rate into the chamber via a first nozzle, the first nozzle may be provided on the chamber above a center region of the wafer.

Also, when the (b) forming step is attained by starting supply of the reaction gas at the second flow rate into the chamber via second nozzles, the second nozzles may be provided on side walls of the chamber above the wafer.

### **Brief Description of the Drawings**

Figs. 1A to 1E are timing charts showing operation timings in the present invention;

10. Figs. 2A to 2E are timing charts showing operation timings in a conventional method;

Fig. 3 is a diagram showing the structure of a plasma CVD apparatus;

15 Fig. 4 is a diagram showing a relation of gate current and accumulated failure percentage in transistors formed by the present invention; and

Fig. 5 is a diagram showing a relation of gate current and accumulated failure percentage in transistors formed by the conventional method.

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### **Description of the Preferred Embodiments**

A film forming method of the present invention will now be described below in detail with reference to the attached drawings.

25 Fig. 3 illustrates the structure of an HDP-CVD apparatus. Referring to Fig. 3, the plasma CVD apparatus in this embodiment is composed of a reaction

chamber formed of ceramic material in the form of a dome. A source coil 25 is wound in an upper side portion of the chamber. When the power is applied from a high frequency power source 19 to the source  
5 coil 25, a source plasma is generated. A stage 23 is provided in a lower portion of the chamber and a wafer 26 is mounted on the stage 23. The stage 23 has an electric static chuck (ESC) and when bias power is supplied from a bias power source 20 to the stage 23,  
10 the plasma film forming process is started using the source plasma. A portion of the bottom of the chamber is provided with an exhaust port 24 connected to a turbo molecular vacuum pump (TMP). A gas nozzle 21 is provided on the top portion of the chamber above the  
15 center portion of the stage 23 to feed a reaction gas at a small flow rate. A plurality of gas nozzles 22 are provided on the side portion of the chamber on positions lower than the source coil 25 but upper than the wafer 26 such that the reaction gas can be  
20 supplied at a large flow rate from the peripheral portion of the wafer 26 on the stage 23. Each of the gas nozzles 22 is directed to the center portion of the wafer 26.

$\text{SiH}_4$  gas as the reaction gas is supplied from  
25 the nozzle 21 to the chamber through a mass flow controller (MFC) 7, a valve 10 and pipe 1.  $\text{O}_2$  gas is supplied from the nozzle 21 to the chamber through a



mass flow controller (MFC) 8, a valve 11 and pipe 2. Ar gas is supplied from the nozzle 21 to the chamber through a mass flow controller (MFC) 9, a valve 12 and pipe 3. SiH<sub>4</sub> gas as the reaction gas is supplied from the nozzle 22 to the chamber through a mass flow controller (MFC) 13, a valve 16 and pipe 4. O<sub>2</sub> gas is supplied from the nozzle 22 to the chamber through a mass flow controller (MFC) 14, a valve 17 and pipe 5. Ar gas is supplied from the nozzle 22 to the chamber through a mass flow controller (MFC) 15, a valve 18 and pipe 6.

Figs. 1A to 1E are timing charts showing the operation timings when gases are introduced and power is applied, in the embodiment of the present invention. The procedure for forming an oxide film will be carried out as shown in the timing charts of Figs. 1A to 1E.

After the wafer 26 is disposed on the stage 23 within the chamber, the chamber is supplied simultaneously at the timing T1 with the O<sub>2</sub> gas via the pipes 2 and 5, and the Ar gas is supplied via the Ar gas pipes 3 and 6, as shown in Figs. 1C and 1D. When the flow rates of these gases enter in stable states, high frequency power is applied from the high frequency power source 19 to the source coil 25 to generate a plasma in the chamber at the timing T2 as shown in Fig. 1E. The generated plasma increases the

temperature of the wafer 26 in a range of 200 to 400 °C. When the temperature of the wafer 26 reaches a temperature of 200 to 400 °C, SiH<sub>4</sub> gas is introduced into the chamber through the SiH<sub>4</sub> gas pipe 1 at the timing T3 as shown in Fig. 1A. Then, the SiH<sub>4</sub> gas is introduced into the chamber through the SiH<sub>4</sub> gas pipe 4 at the timing T4, 1 to 10 seconds after the supply of the SiH<sub>4</sub> gas through the pipe 1 as shown in Fig. 1B.

The bias power is applied from the high frequency power source 20 to the stage 23. At this time, the application of the bias power is carried out at a timing between the introduction of the SiH<sub>4</sub> gas from the SiH<sub>4</sub> gas pipe 1 to the chamber and the introduction of the SiH<sub>4</sub> gas from the SiH<sub>4</sub> gas pipe 4 to the chamber, or after the introduction of the SiH<sub>4</sub> gas from the SiH<sub>4</sub> gas pipe 4 to the chamber.

The flow rates of the SiH<sub>4</sub> gases from the SiH<sub>4</sub> gas pipes 1 and 4 are controlled to different values by the mass flow controllers 7 and 13 which are controlled by a controller (not shown). Particularly, the gas flow rate in the SiH<sub>4</sub> gas pipe 1 is used such that a uniform film can be formed on the wafer 26 when the film thickness is equal to or less than 10 nm. That is, the gas flow rate in the SiH<sub>4</sub> gas pipe 1 is set to an appropriate value between one fifth and one tenth of that in the SiH<sub>4</sub> gas pipe 4. More specifically, the gas flow rate in the SiH<sub>4</sub> gas pipe 1

is 10 SCCM and the gas flow rate in the  $\text{SiH}_4$  gas pipe 4 is 70 SCCM.

As described in the embodiment, by feeding the  $\text{SiH}_4$  gas from the gas pipe having the mass flow controller 7 at a small flow rate into the chamber via the gas nozzle 21, the film can be uniformly formed initially from the center region of the wafer 26 above which the gas nozzle 21 is provided, to the periphery of the wafer 26, while the film has the thickness of 10 nm or less. Thereafter, by feeding the  $\text{SiH}_4$  gas from the gas pipe into the chamber via the gas nozzle 22, the film can be rapidly formed. Thus, it is possible to reduce the ununiformity due to the formation of the film from the peripheral portion of the wafer at the initial film forming step.

In such a manner, when the oxide film is firstly formed on the center region of the wafer 26 at an initial film forming step, the deterioration of the insulating breakdown of a gate oxide film can be avoided because an amount of injected charges into the wafer become uniform at the initial film forming step.

Fig. 4 illustrates gate voltages and accumulated failure percentage in transistors each having an oxide film formed in such a manner, when the wiring lengths are 320  $\mu\text{m}$ , 20320  $\mu\text{m}$ , 80320  $\mu\text{m}$  and 320320  $\mu\text{m}$ , respectively. In general, a gate leak current is  $10^{-12}$  A or less in case of the gate voltage

of 2.5 V. In the gate oxide film formed by the method according to the present invention, it would be understood that the deterioration of the breakdown voltage of the gate oxide film is remarkably improved, as compared with that of the transistors formed in accordance with the conventional method as shown in Figs. 2A to 2E.

In the above embodiment, a large amount of gas is supplied from the gas nozzle 22 into the chamber with the delay of 1 to 10 seconds after the supply of a small amount of gas from the gas nozzle 21 into the chamber. The delay time that is shorter than 1 second or longer than 10 seconds is not suitable. When the delay time is shorter, the film formation is commenced from the peripheral region of the wafer. On the other hand, when the delay time is longer, the characteristic of the initial oxide film is deteriorated and thus the insulating breakdown of the oxide film occurs.

In the above mentioned embodiment, there has been described about the case that a small amount of  $\text{SiH}_4$  gas is fed to the center region of the wafer 26 via the gas nozzle 21. However, if the gas nozzle 21 is slightly displaced from the center region of the wafer 26, it was found that the breakdown voltage of the gate oxide film could be significantly improved, as compared with that of the conventional gate oxide

film as shown in Fig. 5.

As mentioned above, according to the present invention, semiconductor elements in which the breakdown voltage of agate oxide film is not  
5 deteriorated can be provided by feeding a small amount of gas prior to the feeding a large amount of gas in such a manner that the film formation is commenced from the center region of the wafer.

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